ABSTRACT

A gated clock recovery circuit is disclosed that receives an input data stream and generates a frequency and phase aligned clock output. The gated clock recovery circuit substantially instantaneously adjusts the generated clock signal to phase changes in the incoming data stream. In addition, the gated clock recovery circuit generates the clock output signal using only transmitted non-predetermined data. The gated clock recovery circuit includes two PLL circuits. The first PLL (PLL1) adjusts to the frequency of the transmitter, and provides a bias voltage, CAP1, to the second PLL (PLL2) to indirectly initially tune the second PLL (PLL2). The bias voltage, CAP1, is applied to the second (PLL2) through a transmission gate (or switch) that is initially in a closed (short) position. Thus, the first PLL (PLL1) drives the bias voltage, CAP2, of the second PLL (PLL2), to align the frequency with the transmitter, until received data opens the transmission gate. Thereafter, the bias voltage, CAP2, is removed and the second PLL (PLL2) can operate without being controlled by PLL1 so that the second PLL (PLL2) oscillates in phase with the received data. Simultaneously, the received data starts the oscillator in the second PLL (PLL2) so that the second oscillator is in phase with the received data. The second PLL (PLL2) then maintains this phase relationship between the second oscillator and the received data.